Restriction Requirement

In response to the restriction requirement set forth in the Office Action dated December 12, 2001, Applicant hereby affirms the previous election of Invention I, claims 1-13 and 23-24, for prosecution on the merits. Applicant's election is made without prejudice and without traverse.

Drawings

The drawings are objected to. Fig. 2 is amended in the attached sheet to delete reference numeral 10, as suggested by the Examiner. A clean replacement sheet is also provided. Withdrawal of the objection is respectfully requested.

Specification

The specification is objected to because of informalities. The specification is amended herein as suggested by the Examiner. Withdrawal of the objections is respectfully requested.

Please notice that pages 13 and 14 were expressly not a part of the patent application as originally submitted, but rather were provided for the Examiner's convenience.

Claims

Claims 14-22 are withdrawn from consideration by the Examiner pursuant to Applicant's election. Claims 14-22 are not canceled. Claim 5 is canceled. Claims 1, 6, and 7 are amended, and Claims 2-4 and 8-24 remain as filed.

Applicant thanks the Examiner for the clear statement of grounds for rejection. Before addressing individually the specific grounds stated by the Examiner, Applicant wishes to briefly point to some substantial differences which Applicant believes distinguish the present invention over the prior art cited.

Applicant acknowledges some substantial similarities between the subject matter of the present application and that of the *Lee* '049 reference cited by the Examiner. However, Applicant respectfully avers that *Lee* does not teach, and indeed teaches away from, at least one important aspect of the present invention. It should be noted that, despite an apparent similarity in the drawings of the *Lee* '049 patent and the present application, there is a very substantial difference in

relative scale. The *Lee* '049 patent is directed to the defining of "dummy REGIONS" (emphasis added) to be formed within isolating regions which surround functional regions on a chip. However, the present application is directed to the addition of "traces" (52, 64, 74) in and among the traces of the actual functioning circuitry. Perhaps this difference in emphasis is partially explained by the fact that the present invention is intended primarily (although not necessarily exclusively) for application to liquid crystal on silicon ("LCOS") display arrays, wherein the active circuitry covers most of the central area of the chip, and further wherein attention to flatness is much more critical even than in an ordinary semiconductor. In support of this point, please notice Fig. 3 of the *Lee* '049 patent, and the text beginning at column 4, line 43. Notice that the "real active pattern region 21" is shown as a simple rectangular box (as are the "dummy active pattern regions 30"). Of course, in actual practice, there will be a complex pattern of circuitry within that "real active pattern region 21" box. That fact is most relevant to the present invention, but is not at all relevant to the *Lee* '049 disclosure and is, therefore, quite properly omitted from that disclosure. Please notice that, while the *Lee* drawings generally show an entire chip (or at least a substantial portion of a chip), in order to illustrate the present invention, it was necessary to show only a very small portion of the circuitry of a chip in each of the drawings.

As stated above, there is some similarity between the two procedures. Briefly, the *Lee* '049 patent teaches the "growing" of regions (by extending the dimensions of the region) about a real active pattern region, such regions to be defined as "dummy active pattern regions 30". Although there are differences in detail, the present application does describe the defining of "fill areas 38" surrounding "functional circuitry areas 40". Please notice that there is no equivalent to the presently described process for defining the functional circuitry area 40 in the *Lee* '049 reference, since the real active pattern regions 21 (Fig. 3 of *Lee*) are inherently obvious, or are at least presumed to be so in the *Lee* disclosure.

In summary on this point, despite some superficial similarities, the *Lee* '049 patent simply does not teach, or even suggest, any way to fill in traces among the traces of an "active pattern region". Nor could the *Lee* method be adapted for such use.

Before proceeding to a discussion of the specific amendments made to the claims herein, please notice what the inventor believes to be the most distinguishing characteristic of the present invention. That is, the nature of the "fill pattern" (that is, the pattern which is used to fill the area

defined as needing filling). Again, there is little or no discussion at all regarding what sort of pattern is to be used to fill the "dummy active pattern regions 30" in the *Lee* disclosure. The present inventor believes that all such "fill" in the prior art has always consisted of simple iterative patterns (blocks, lines, even swastikas, and the like). According to the present invention, the "fill pattern" is selected from functional circuitry near the area where the fill pattern is to be placed. An example of part of this description is found at page 5, line 8 of the present application:

> According to the present invention, the fill metal traces 52 of the metal fill pattern 50 will be selected to be alike to adjacent functional circuitry (not shown) which might lie adjacent or near to the portion of the example metal layer 30 (Fig. 3) on which the functional circuitry 32 of Fig. 3 is found. In the example presently described, the metal fill pattern 50 is selected from the metal traces of the particular metal layer 14, 16, 18 or 20 on which the metal fill pattern 50 is to be used. As will be discussed in more detail hereinafter, should there be substantial gaps in such metal fill pattern 50 it will be an option of the operator to add metal to complete the metal fill pattern 50.

The fill pattern is selected from nearby circuitry on the theory that such a fill pattern will probably be more like the surrounding circuitry than will be any abstract or arbitrarily selected fill pattern. Note that the present application does provide for the addition of additional pattern portions where there is a substantial gap in the pattern selected from the actual functioning circuitry. As discussed in the application, this optional additional step is presently accomplished by operator intervention.

Regarding Claim Rejections under 35 USC §102:

Applicant acknowledges that Claim 1, as originally drafted, might not have sufficiently distinguished the invention over the prior art. Therefore, Applicant has included all of the limitations of original Claim 5 in the amended Claim 1.

Regarding the Examiner's rejection of Claim 5 (page 7, line 5 of the Office Action) the Examiner asserts that:

> *Lee* inherently provides the dummy fill pattern as an example of an alternative functional circuitry, since the basis of establishing the dummy fill pattern is founded upon dimensions emanated from the existing circuitry.

Applicant respectfully avers that the subtractive process of *Lee* defines regions only, and could not be used to define a pattern to fill such regions. There is no teaching in *Lee* regarding the pattern to be used to fill the regions defined by the *Lee* invention. Although it is not specifically stated, Applicant believes that the intention of the *Lee* teachings is to completely fill the regions defined

according to the *Lee* invention, rather than to fill the region with a "pattern" fill. Alternatively, the *Lee* invention could certainly be used to define regions to be filled by a pattern. However, the *Lee* disclosure does not discuss what pattern might be used. It is difficult to understand exactly how the pattern of the working circuitry would be duplicated by just extending the dimensions of the circuitry area. Indeed, such a process would be entirely inapplicable to open spaces within the greater active circuitry error.

Regarding the Examiner's rejection of Claim 33 (page 8, line 12 of the Office Action): While the Applicant agrees that a dummy fill area is defined in *Lee* (by enlarging the "real active pattern region" by a first amount, then by a second smaller amount, and then by subtracting the smaller newly defined region from the first larger newly defined region, this process defines only a region to be filled. Applicant respectfully disagrees that there is anything in this teaching that either inherently or specifically discusses what pattern should be used to fill this region.

Regarding Claim Rejections under 35 USC §103:

Applicant respectfully disagrees with the Examiner's assertion to the effect that one skilled in the art could reasonably infer the fill pattern selection method described and claimed in the present application from the teachings of *Lee*. Indeed, because, to the Applicant's knowledge, no one in the prior art has used an example of nearby real active circuitry as a template for a fill pattern, there would have to be at least some teaching or suggestion in the prior art to lead one skilled in the art to such an inference. Indeed, there is no such teaching at all to be found in *Lee* '049.

CONCLUSION

Applicant fully understands how, after first reading Applicant's disclosure, the region definition process of *Lee* could be misunderstood to refer to the trace fill pattern method presently described and claimed. Indeed, upon Applicant's first reading of the *Lee* '049 reference the above described important distinctions were not immediately clear. However, Applicant believes that the Examiner will agree, upon rereading *Lee*, that *Lee* does not teach or suggest using "an example of an alternative functional circuitry" as a fill pattern, as recited in amended Claim 1.

SUMMARY

Claims 14 through 22 have been withdrawn from consideration by the Examiner. Claim 5 has been deleted. Claims 1 through 4, 6 through 13, 23 and 24 remain in this application. Claim 1 has been amended to include all of the limitations of the former Claim 5. Applicant respectfully requests that the Examiner reconsider the stated grounds for rejection of the former Claim 5 and Claim 23. The remaining dependant Claims should now be allowable at least as further limitations on the independent Claims 1 and 23, and further by virtue of their specifically recited limitations in combination with the limitations of their respective base claims. It is now thought that this application is in complete condition for allowance, and such action is respectfully requested. Applicant urges the Examiner to call Applicant's undersigned counsel should there be any remaining issues, or if the Examiner has any suggestions for expediting the prosecution of this application.

Respectfully submitted,

HENNEMAN & SAUNDERS

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Date: 4/17/03

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CERTIFICATE OF MAILING (37 CFR 1.8(A))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231.

Date: 4/17/03

Larry E. Henneman, Jr.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wang, Xiaojun
Serial No: 10/017,458
Filing Date: 12/12/2001

Docket No: 0011-051
Group Art Unit: 2824
Examiner: Michael K. Luhrs

IMPROVED DUMMY METAL PATTERN METHOD AND APPARATUS

Version With Markings to Show Changes Made

IN THE SPECIFICATION

Please amend the Specification, as shown in the attached "Version With Markings To Show Changes Made," to read as follows:

The heading at page 12, line 1:

[ABSTACT] ABSTRACT

The paragraph beginning at page 3, line 28:

An example of the present invention is a method for producing dummy metal patterns shown in the flow diagram of Fig. 1, and designated therein by the general reference character 10. Fig. 2 is a side elevational, partially cross sectional diagrammatic (not to scale) view of a small portion of a reflective LCOS array 11, such as might employ the present inventive method and construction. The reflective LCOS array 11 has, not unlike conventional prior art devices, a plurality of material layers 12. The embodiment discussed by way of example herein has a mirror layer 14, a first metal (M1) layer 16, a second metal (M2) layer 18, and a third metal (M3) layer 20. In the present example also are a poly (recrystallized silicon) layer 22 and a diffusion layer 24. One skilled in the art will recognize that where traces on the poly layer 22 mask those of the diffusion layer 24 are semiconductor junctions 26. Also visible in the view of [Fig. 1] Fig. 2 are a plurality of silicon dioxide insulating layers 28.

The paragraph beginning at page 6, line 9:

In a fill partially filled areas operation 58, areas such as the circuitry area 29, discussed above, are filled. As discussed previously herein, the margin area 34 (Fig. 3) is grown around the functional circuitry 32 in a grow margin area operation 59. In a trim dummy to margin operation 60 (Fig. 1) the fill metal traces 52 (Fig. 5) are trimmed to eliminate overlap with the functional circuitry area 40 (Fig. 4). This will leave a first trimmed fill pattern 62 as seen in the diagram of Fig. 6. The first trimmed fill pattern 62 has trimmed metal traces 64 which are located only overlying the fill area 38 of Figs. 3 and 4 and, in this example, the unfilled area 31 (Fig. 3). In the example of Fig. 5, it can be seen that the first trimmed metal traces 64 has a metal sliver 66 which is left where trimming away the functional circuitry area 40 (Fig. 4) leaves only a thin portion of the fill metal traces 52 (Fig. 5) behind.

The paragraph beginning at page 6, line 27:

Fig. 8 is an example of a completed metal trace pattern 76. The completed metal trace pattern 76 is created in an overlay functional and dummy patterns operation 78 (Fig. 1) by combining the functional circuitry 32 with the second trimmed metal traces 74. According to the present invention, the surface of the circuitry area 29 and the unfilled area 31 [(Fig. 2)] (Fig. 3) are filled in with patterns which general resemble the functional circuitry 32 [(Fig. 2)] (Fig. 3) thereabout.

The paragraph beginning at page 5, line 7:

Fig. 5 is an example of a portion of a metal fill pattern 50. The metal fill pattern 50 has a plurality of fill metal traces 52 separated by unfilled space 54. According to the present invention, the fill metal traces 52 of the metal fill pattern 50 will be selected to be alike to adjacent functional circuitry (not shown) which might lie adjacent or near to the portion of the example metal layer 30 (Fig. 3) on which the functional circuitry 32 of Fig. 3 is found. In the example presently described, the metal fill pattern 50 is selected from the metal traces of the particular metal layer 14, 16, 18 or 20 on which the metal fill pattern 50 is to be used. As will be discussed in more detail hereinafter, should there be substantial gaps in such metal fill pattern 50 it will be an option of the operator to add metal to complete the metal fill pattern 50. [While it is conceivable that an algorithm might be developed to automatically complete the metal fill pattern

50, in] In the embodiment of the invention described herein [such operation] the metal fill pattern 50 is completed [is performed] by a visual inspection and operator intervention, as will be discussed in relation to the inventive method hereinafter. It is within the scope of the invention that the metal fill pattern could also be completed using a more automated method, according to either a known algorithm or another yet to be developed.

The paragraph beginning at page 7, line 2:

One skilled in the art will recognize that the operations 59, 60, 70 and 78 can be repeated for each different circuitry area 29 to be filled in according to the present inventive method 10. Similarly, [In] in the fill unfilled areas operation 57 as many iterations of the metal fill pattern 50 as necessary to fill the existing quantity of unfilled areas 31 can be used. The quantity of iterations of the inventive method 10 and each step thereof will be peculiar to the particular application.

The paragraph beginning at page 7, line 20:

The inventive method for creating dummy fill metal patterns 10 is intended to be widely used in the production of integrated circuits, and in particular video imaging devices, especially where the size and/or criticality of the display requirements call for minimal distortion and optimal image clarity and resolution. The present inventive method is potentially applicable to any metal (circuitry) layer of the array stack. However, [it is thought] the inventor believes it to be more useful and necessary the closer such level is to the top layer, wherein reduction of physical distortion is most critical, although the inventor acknowledges that other authorities have proposed that such correction is most critical in the lower levels.

Pages 13 and 14:

IN THE CLAIMS

1. (Amended) A method for creating a dummy metal fill pattern near functional circuitry, comprising:

a. creating a margin area around the functional circuitry;

b. trimming a dummy fill pattern to the margin area to create a trimmed fill pattern; and

c. overlaying said trimmed fill pattern and the functional circuitry; and

wherein the dummy fill pattern is an example of an alternative functional circuitry.

6. (Amended) The method for creating a dummy metal fill pattern of claim [5] 1, wherein:

the alternative functional circuitry is selected to be alike to that near the functional circuitry.

7. (Amended) The method for creating a dummy metal fill pattern of claim [5] 1, wherein:

the alternative functional circuitry is a selected portion of functional circuitry from a metal layer on which the dummy metal fill pattern is to be used.

Respectfully submitted,

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